MP2672

Boost Charger with Cell Balance for 2-cell in series Lithium-ion Battery

The Future of Analog IC Technology

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MP2672 is a high-integrated, flexible switch-mode battery charge IC for Lithium-ion battery with 2 cells in series which is used in a wide range of portable applications.

When the input power supply is present, the MP2672 operates in boost mode to charge the battery with 2 cells in series. When the charging is enabled, MP2672 automatically detects the battery voltage and charges the battery in the three phases: pre-charge, constant current charge and constant voltage charge. Other features include charge termination and auto-recharge.

The MP2672 also has narrow voltage DC (NVDC) power structure. When battery is weak, MP2672 regulates the system output at minimum voltage level to power the system instantly and charge battery via battery FET simultaneously.

The MP2672 also has cell-balance function. It will always monitor voltage across each cell and equalize cell voltages once the difference exceeds the mismatch threshold.

The MP2672 has two configuration modes, standalone mode and host-control mode. In standalone mode, the charging parameters can be configured by hardware pins. While in host-control mode, the charging parameter can be configured by I^2C registers.

The MP2672 has diversified and robust protections. It has thermal regulation loop to decrease the charge current in case the junction temperature exceeds the thermal loop threshold. It also has battery temperature protection compliant to the JEITA standard. Other safety features include input over-voltage protection, battery over-voltage protection, thermal shutdown, battery temperature monitoring, watchdog timer and a programmable back-up timer to prevent prolonged charging of a dead battery.

FEATURES

- 4.0V-to-5.75V Input Operation Voltage
- Up to 14V Sustainable Voltage
- Up to 2A Programmable Charge Current for Battery with 2 cells in Series
- Compatible with Host-control and Standalone Mode
- NVDC Power Path Management
- Programmable Input Voltage Limit
- Programmable Charge Voltage with 0.5% Accuracy
- No External Sense Resistor Required
- Integrated Cell Balancing Circuit for Cell Mismatch
- Preconditioning for Fully Depleted Battery
- Flexible New Charging Cycle Initiation
- Charging Operation Indicator in Standalone Mode
- Missing Battery Detection in Host-control Mode
- I^2C Port for Flexible System Parameter Setting and Status Reporting in Host-control Mode
- Negative Temperature Coefficient Pin for Temperature Monitoring Compliant to JEITA Standard
- Built-in Charging Protection and Programmable Safety Timer
- MOSFET Cycle-by-Cycle Over Current Protection
- Thermal Regulation and Thermal Shutdown
- 2mmx3mm QFN-18 package

APPLICATIONS

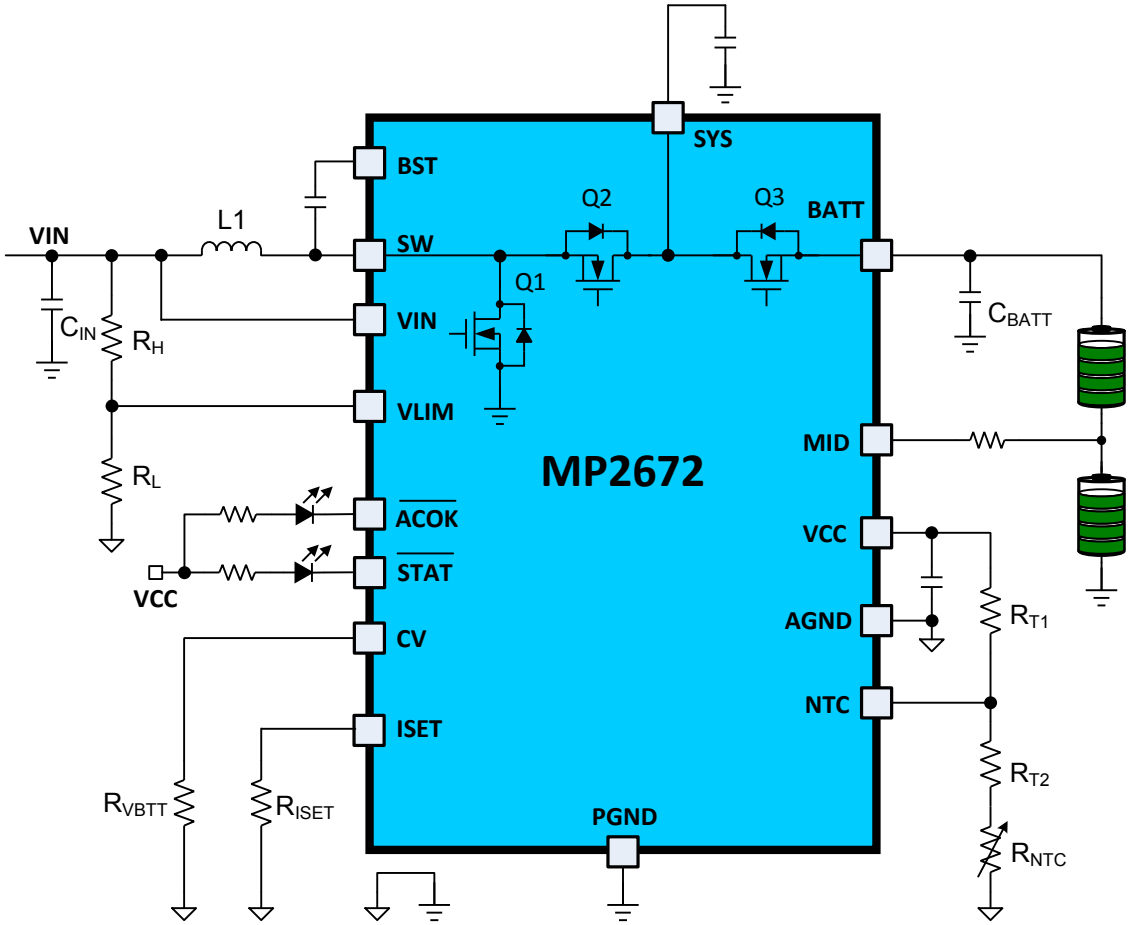
- Portable Hand-held Solutions
- POS Machine
- Blue-tooth Speaker
- E-Cigarette
- General 2-Cell Application

TYPICAL APPLICATION

Standalone Mode:

Connect CV pin to AGND via a resistor. Set the battery full voltage according to below table.

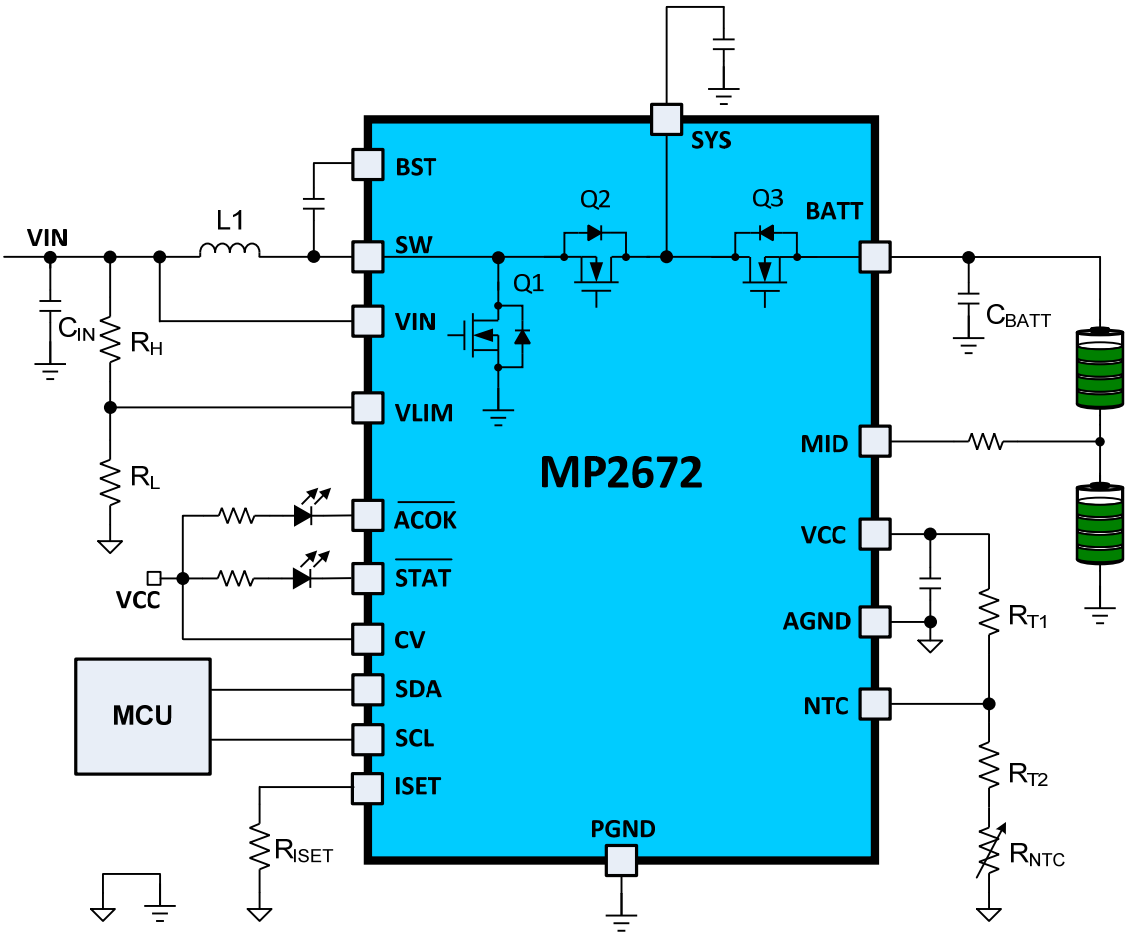
R_{VBATT} Range	V_{BATT_REG}
30kΩ	8.4V
75kΩ	8.6V
105kΩ	8.7V
135kΩ	8.8V



TYPICAL APPLICATION

Host-control Mode

Connect CV pin to VCC. Set the battery full voltage according to the register.



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2672GD-xxxx**	QFN-18 (2mmx3mm)	*See Below*

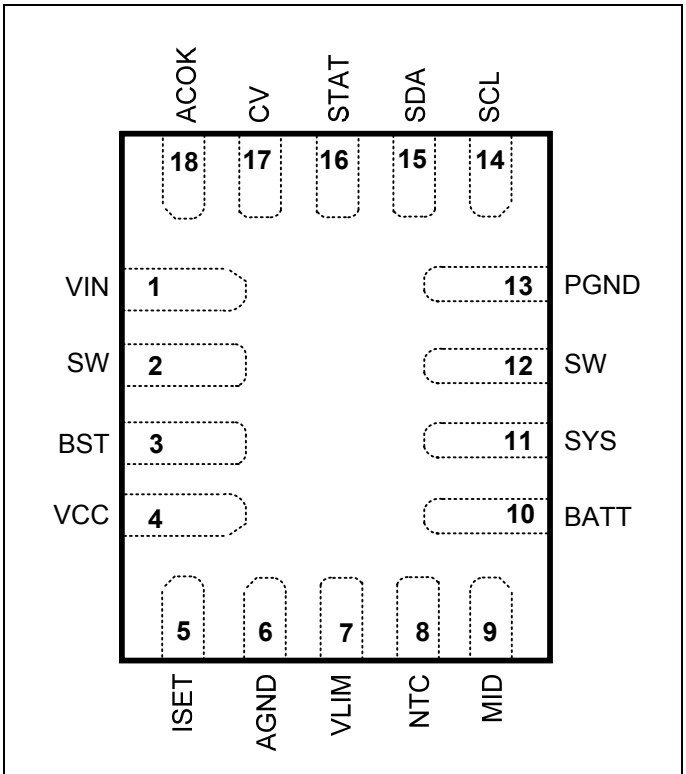
*For Tape & Reel, add suffix –Z (e.g. MP2672GD–xxxx-Z)
**"xxxx" is the register setting option. The factory default is "0000". This content can be viewed in the "I^{2}C REGISTER MAP" section. For customer options, please contact an MPS FAE to obtain a "xxxx" value.

TOP MARKING

BHA
YWW
LLL

Y: year code
WW: week code
BHA: part number
LLL: lot number

PACKAGE REFERENCE



QFN-18 (2mmx3mm)

PIN FUNCTIONS

Package Pin #	Name	Type	Description
1	VIN	I	Input voltage sense pin and power supply for VCC LDO.
2, 12	SW	Power	Switching Node. Middle point of the high-side and low-side FET of the boost.
3	BST	Power	Bootstrap. Connect a bootstrap capacitor between BST and SW to provide a floating supply to the high-side FET driver.
4	VCC	Power	Internal LDO output pin. Bypass a 2.2μF ceramic capacitor from this pin to AGND. Recommend pull no more than 30mA current from this pin.
5	ISET	I	Connect an external resistor to GND to program the charge current, which also limit the maximum charge current in Host-control mode.
6	AGND	I/O	Analog ground.
7	VLIM	I	Input Voltage Limit feedback pin. Connect a resistive divider from VIN to AGND to program the minimum input voltage limit threshold.
8	NTC	I	Battery Temperature Sense Input. See NTC protection section.
9	MID	I/O	Middle point of the high-side and low-side cell. Used to measure the voltage and provide balance path for each cell.
10	BATT	Power	Battery positive terminal. Connect a 22μF capacitor from BATT to PGND as close as possible to the IC.
11	SYS	Power	System Output. Connect a 2×22μF capacitor from SYS to PGND as close as possible to the IC.
13	PGND	Power	Power ground.
14	SCL	I/O	I^2C Interface Clock Pin. Not valid if CV pin is connected to VCC.
15	SDA	I/O	I^2C Interface Data Pin. Not valid if CV pin is connected to VCC.
16	$\overline{\text{STAT}}$	I/O	Open-drain indicator for charging operation. Also can be used as INT in Host-control mode.
17	CV	I	Pull CV to VCC to configure IC to host-control mode. Connect an external resistor to GND to configure IC to standalone mode and program the battery full voltage via the resistor value.
18	$\overline{\text{ACOK}}$	O	Open-drain Input Supply Indicator. It's an open-drain output. It is pulled to Low when input voltage is higher than $V_{IN\ UVLO}$ and $V_{IN\ OVLO}$.

ABSOLUTE MAXIMUM RATINGS (1)

BATT.....-0.3V to +14V
SW, ...-0.3V (-2V for 50ns) to +14V
SYS.....-0.3V to +14V
MID, VIN .....-0.3V to +12V
BST to SW…….....-0.3V to +5V
All Other Pins to GND.....-0.3V to +5V
Continuous Power Dissipation.....(T_A=+25°C)(2)
..... 1.78W
Junction Temperature.....150°C
Lead Temperature (Solder).....260°C
Storage Temperature…. ..... -65°C to +150°C

Recommended Operating Conditions (3)

VIN to GND…….. 4V to 5.75V
BATT to GND..... up to 9V
I_{CHG}..... up to 2A
I_{DSCHG}.....Up to 3A
I_{SYS} .....Up to 2.5A
Operating Junct. Temp. (T_J)..... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN2x3	70	15	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Power Characteristics						
Input Over-voltage Lock-out Threshold	V_{IN_OVLO}	V_{IN} rising	5.75	6.0	6.25	V
Input Over-Voltage Lock-out Threshold Hysteresis				150		mV
Input Under-voltage Lock-out Threshold	V_{IN_UVLO}	V_{IN} falling	3.35	3.55	3.75	V
Input Under-voltage Lock-out Threshold Hysteresis				150		mV
Boost Converter						
Input Quiescent Current	I_{IN_Q}	Battery and system are float, Charging is enabled			2.5	mA
VCC LDO Output	V_{VCC}	V_{IN}=5V, I_{VCC}=20mA	TBD	3.6	TBD	V
Low Side NFET On Resistance	R_{ON_Q1}			60	80	mΩ
High Side NFET On Resistance	R_{ON_Q2}			30	40	mΩ
Peak Current Limit for Low-side NFET	I_{LS_PK}	Step-up Mode	6	7		A
Valley Current Limit for High-side NFET	I_{HS_VL}	Step-up Mode	5	6		A
Operating Frequency	F_{SW}	REG07 Bit[7]=1	TBD	1200	TBD	kHz
System Regulation Minimum Voltage (V_{BATT_PRE}+V_{TRACK})	V_{SYS_MIN}	REG00Bit[3:1]=000, REG00Bit[0]=0, V_{BATT}=5V	TBD	6.2	TBD	V
		REG00Bit[3:1]=100, REG00Bit[0]=0, V_{BATT}=5V	TBD	6.6	TBD	
		REG00Bit[3:1]=111 REG00Bit[0]=1, V_{BATT}=5V	TBD	7	TBD	
Battery Track Regulation Voltage	V_{TRACK}	REG00 Bit[0]=0		200		mV
		REG00 Bit[0]=1		300		
Battery Charger						
Pre Charge Threshold	V_{BATT_PRE}	REG00 Bit [3:1]=000	TBD	6.0	TBD	V
		REG00 Bit [3:1]=100	TBD	6.4	TBD	
		REG00 Bit [3:1]=111	TBD	6.7	TBD	
Pre Charge Threshold Hysteresis		V_{BATT} falling		175		mV
Pre Charge Current	I_{PRE}		80	100	120	mA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Fast Charge Current	I_{CC}	Host-control mode, REG01Bit[3:0]=1111, R_{ISET}=24kΩ, Standalone mode, R_{ISET} = 24kΩ	0.4	0.5	0.6	A
		Host-control mode, REG01Bit[3:0]=1111, R_{ISET} = 6kΩ, or in standalone mode, R_{ISET} = 6kΩ	1.8	2	2.2	A
Termination Charge Current	I_{TERM}	As the percentage of I_{CC}	5	10	15	%
		If 10%*I_{CC} < 150mA	120	150	180	mA
Input Minimum Voltage Regulation Reference	$V_{IN\_MIN\_REF}$		1.18	1.2	1.22	V
Battery Charge Voltage Regulation	$V_{BATT\_REG\_ACC}$	V_{BATT_REG}=8.3V, Host-control mode, REG00[7:5]=000,	-0.5		0.5	%
		V_{BATT_REG}=8.4V, Host-control mode, REG00[7:5]=001, /Standalone mode, R_{VBATT}=30kΩ				
		V_{BATT_REG}=8.8V, Host-control mode, REG00[7:5]=101, /Standalone mode, R_{VBATT}=135kΩ				
		V_{BATT_REG}=9.0V, Host-control mode, REG00[7:5]=111				
Recharge Threshold below V_{BATT_REG}	V_{RECH}			400		mV
Battery Over Voltage Protection Threshold	V_{BATT_OVP}	As the percentage of the V_{BATT_REG}	102	104	105	%
Battery Over Voltage Protection Hysteresis		As the percentage of the V_{BATT_REG}		1		%
SYS to BATT NFET On Resistance	R_{ON_Q3}			30	40	mΩ
Battery Quiescent Current	I_{BATT_Q}	V_{IN}<V_{IN_UVLO}, V_{BATT}=8.4V, System no load		30		μA
$\overline{ACOK}$, $\overline{STAT}$, pin output low voltage		Sinking 1.5mA			400	mV
$\overline{ACOK}$, $\overline{STAT}$, pin leakage current		Connected to 5V			1	μA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Termination Deglitch Time	t_{TERM_DGL}			200		ms
Recharge Deglitch Time	t_{RECH_DGL}			200		ms
Battery Temperature Monitoring (JEITA)						
NTC Low Temp Rising Threshold	V_{COLD}	As percentage of V_{CC}	68.8	70.8	72.8	%
NTC Low Temp Rising Threshold Hysteresis		As percentage of V_{CC}		2		%
NTC Cool Temp Rising Threshold	V_{COOL}	As percentage of V_{CC}	60.9	62.9	64.9	%
NTC Cool Temp Rising Threshold Hysteresis		As percentage of V_{CC}		2		%
NTC Warm Temp Falling Threshold	V_{WARM}	As percentage of V_{CC}	38.3	40.3	42.3	%
NTC Warm Temp Falling Threshold Hysteresis		As percentage of V_{CC}		2		%
NTC Hot Temp Falling Threshold	V_{HOT}	As percentage of V_{CC}	32.5	34.5	36.5	%
NTC Hot Temp Falling Threshold Hysteresis		As percentage of V_{CC}		2		%
Thermal Regulation and Protection						
Junction Temperature Regulation	T_{J_REG}			120		°C
Thermal Shutdown Temperature(1)	T_{J_SHDN}	Rising Threshold		150		°C
Thermal Shutdown Hysteresis(1)				20		°C
Cell Balance Function						
Internal Balance FET On Resistance	R_{ON_BHS}			2		Ω
	R_{ON_BLS}			2		Ω
Cell Balance Start Voltage Threshold	V_{CELL_BAL}	I^2C programmable, REG01 Bit6=1	3.6	3.7	3.8	V
Cell Voltage High to Low Cell Mismatch Threshold	$V_{CELL\_DIFF\_HTL}$		40	50	60	mV
Cell Voltage Low to High Cell Mismatch Threshold	$V_{CELL\_DIFF\_LTH}$		40	50	60	mV
Balance Threshold Hysteresis				30		mV

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
I²C Communication Interface						
Input High Threshold Level	V_{IH}	$V_{PULL\ UP}$ = 1.8V	1.3			V
Input Low Threshold Level	V_{IL}	$V_{PULL\ UP}$= 1.8V			0.4	V
Output Low Threshold Level	V_{OL}	I_{SINK} = 5mA			0.4	V
I²C Clock Frequency	F_{SCL}				400	kHz
Timing Characteristic						
Clock Frequency	F_{CLK}			130		kHz
Watchdog Timer	t_{WTD}	REG02 [5:4]=01		40		s
Safety Charge Timer	t_{TMR}	I²C programmable, REG02 Bit[2:1]=11		20		Hours

Notes:

5) Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Insert
Performance Curve
Provide Source File
(Excel Data & Chart)
(Format > Picture > Layout > In Front of Text)
Shift-Scale > Alt-Move

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Insert
Performance Curve
Provide Source File
(Excel Data & Chart)
(Format > Picture > Layout > In Front of Text)
Shift-Scale > Alt-Move

FUNCTIONAL BLOCK DIAGRAM

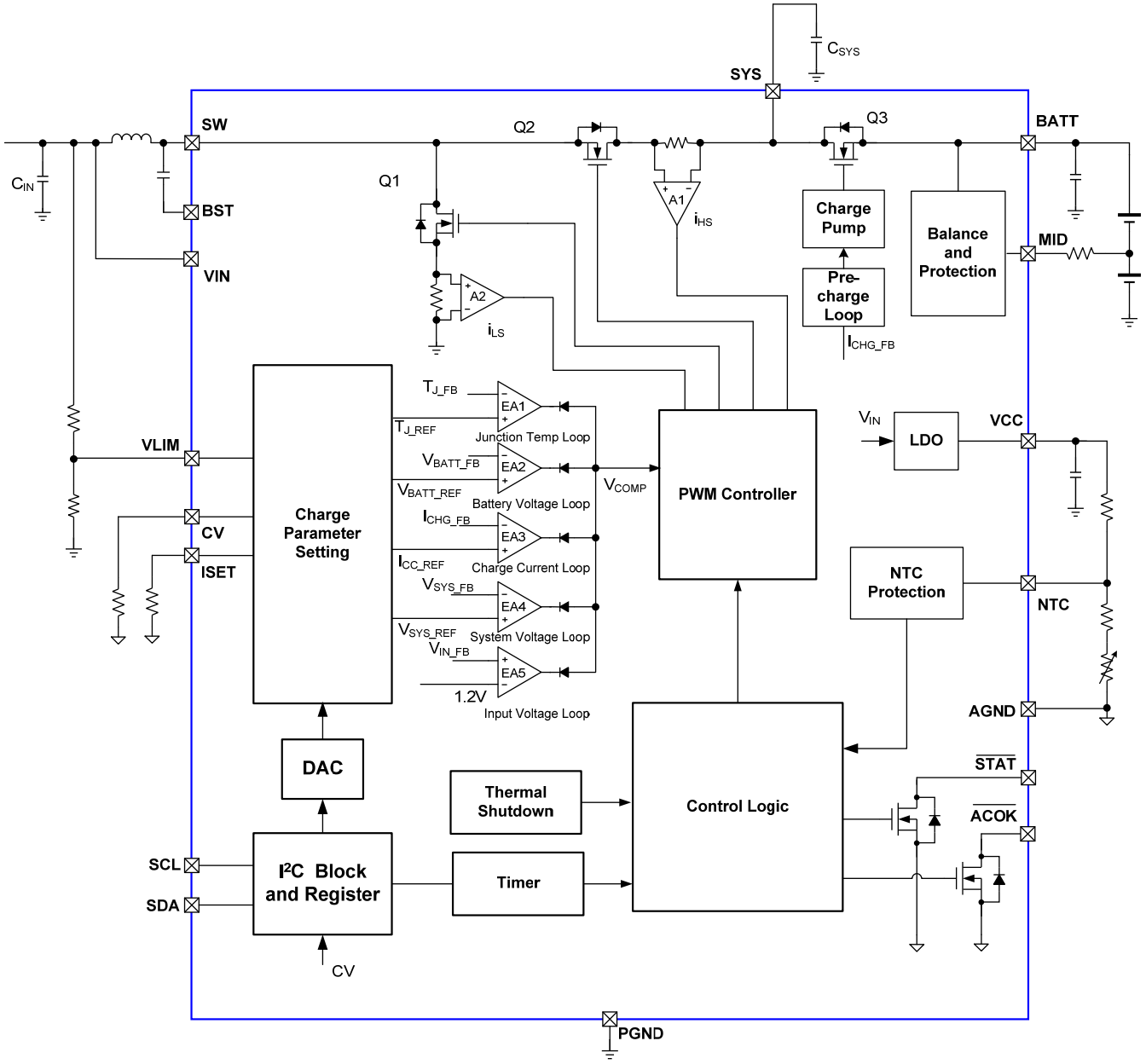


Figure 1 Functional Block Diagram

OPERATION

The MP2672 is a highly integrated switch-mode battery charger to charge Lithium-ion battery with 2 cells in series from 5V input power supply, which could be adapter or USB input.

Host-control Mode and Standalone Mode

MP2672 can operate in either Host-control mode or standalone mode. After input power on, MP2672 checks CV status first.

- If CV is pulled up to logic high, MP2672 will work in host-control mode.
- If CV is connected to ground through a resistor, MP2672 will work in standalone mode.

In host-control mode, charging parameters can be programmable by I^2C registers. In standalone mode, V_{BATT_REG} and I_{CC} can be set by external analog pin.

Table 1: Host-control Mode and Standalone Mode

CV pin	Mode	V_{BATT_REG}	I_{CC}
Connect resistor to GND	Standalone	Set by CV resistor	Set by ISET resistor
Pull up to VCC	Host-control	Set by I^2C register	Set by I^2C register*

*Note: Maximum charge current is limited by ISET setting.

Internal Power Supply

The VCC LDO is powered by input power supply and it is used to power the internal circuit and MOSFET driver. When the input is absent, the VCC LDO will be off. An external capacitor is required to be connected from VCC pin to GND. The VCC output is regulated at 3.6V typically when V_{IN} is 5V. When the VIN is lower than 3.6V, the LDO enters into dropout state and LDO FET is fully turned on. VCC output is not able to carry more than 20mA current load.

Input Voltage vs. System Voltage Limitation

To avoid the MP2672 entering the open-loop operation due to the minimum on time of low-side FET. The boost converter will turn off when $V_{SYS} < 1.1xV_{IN}$, it will restart and check the input voltage and system voltage again. And the boost will turn off again after around 1ms soft-start time if V_{SYS} is still lower than $1.1xV_{IN}$.

As a result it is recommended to choose V_{BATT_PRE} and V_{TRACK} to ensure the minimum output voltage of boost is above the 1.1x the maximum DC input voltage.

Input Power Start-up

When input voltage is lower than V_{IN_UVLO}, SYS is powered by the battery via the Q3, which is fully turned on at this time. When input power is connected, the Q3 will quit fully on mode and enter ideal diode mode when V_{IN} is higher than V_{IN_UVLO}. At the same time the boost starts up with soft-start of the system voltage loop. When the system voltage rises around 20mV higher than the battery voltage the Q3 will be turned off for a while and turn on again with soft-start of charge current after system voltage soft-start completes.

NVDC Power Structure

The MP2672 employs the Narrow VDC (NVDC) power structure which is composed of a frond-end boost converter and a rear-end battery FET between SYS and BATT pin. By doing this it allows the separate control between the system and the battery. The system is given the priority to start up even with a deeply-discharged or missing battery. So when the input power is available even with a depleted battery, the system voltage is regulated at the minimum system voltage V_{SYS_MIN} which is set by I^2C register REG00 Bit [3:1] and REG00 Bit [0].

As shown in Figure 2, for the system voltage control,

(1) When the battery voltage is lower than V_{BATT_PRE}, the system voltage is regulated at $V_{SYS\_MIN} = V_{BATT\_PRE}+V_{TRACK}$ and the battery FET works linearly to charge the battery with pre-charge current.

(2) When the battery voltage is above the V_{BATT_PRE}, the battery FET is fully turned on, the system voltage is always $I_{CHG}\times R_{ON\_Q3}$ higher than the battery voltage. Once the battery charging is completed, the system output (V_{SYS}) is regulated to $V_{BATT} + V_{TRACK}$.

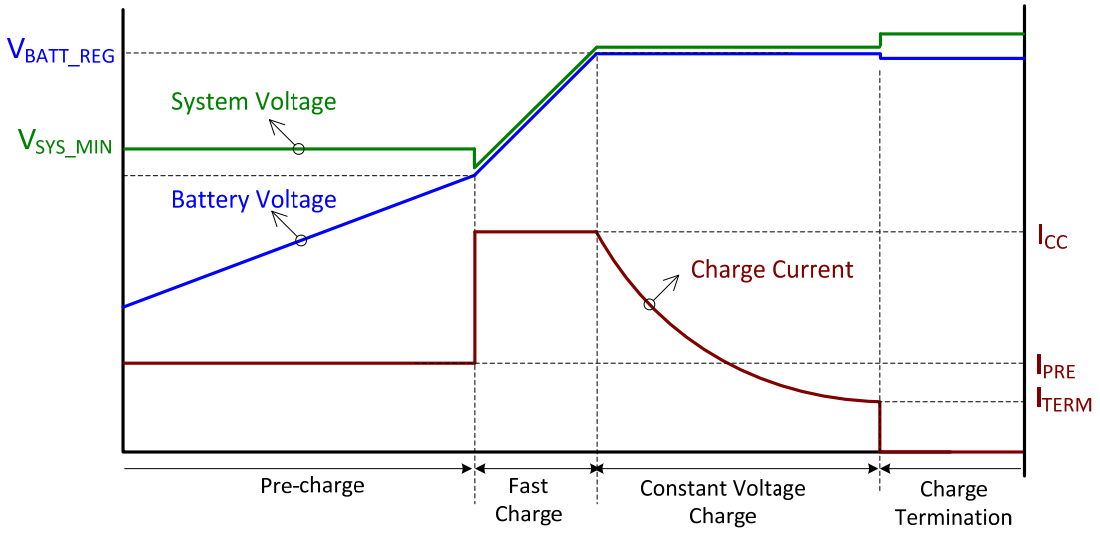


Figure 3 Battery Charge Profile

(3) When charging is disabled, the V_{SYS} is also regulated to V_{TRACK} higher than real battery voltage.

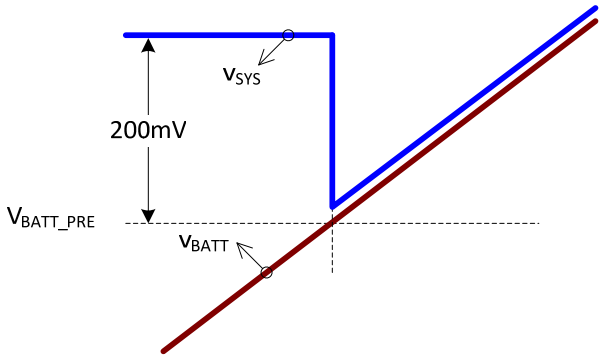


Figure 2 V_{SYS} Variation with V_{BATT}

Battery Charge Profile

As shown in Figure 2, the MP2672 provides three main charging phases: pre-charge, constant-current charge and constant-voltage charge.

Phase 1 (Pre-charge)

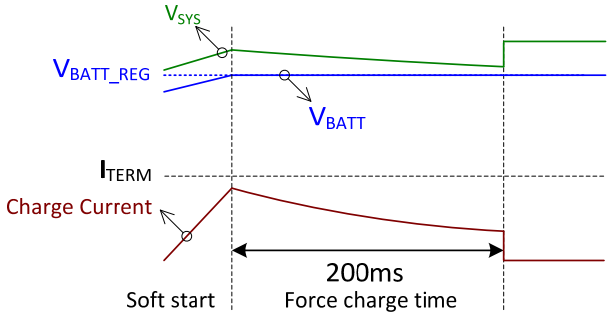
When the battery voltage is lower than the V_{BATT_PRE}, the MP2672 regulates the system voltage at V_{SYS_MIN} and apply a safely pre-charge current I_{PRE} to the deeply depleted battery until the battery voltage reaches pre-charge to fast charge threshold V_{BATT_PRE}. If V_{BATT_PRE} is not reached before pre-charge timer (30 mins) expires, the charge cycle is ceased and a corresponding timeout fault signal is asserted.

Phase 2 (Constant-current charge)

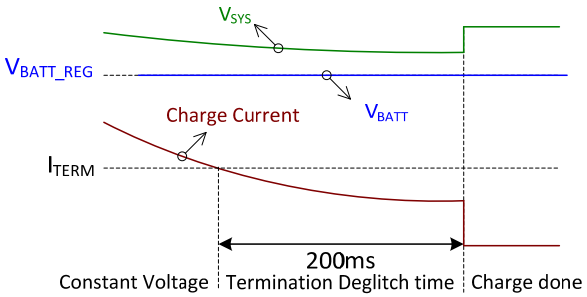
When the battery voltage exceeds V_{BATT_PRE}, the MP2672 stops the pre-charge phase and enters into fast charge phase. The fast charge current can be programmable via ISET pin in standalone mode or I^2C register in host mode.

Phase 3 (Constant-voltage charge)

As depicted in Figure 4, when the battery voltage rises to the battery regulation voltage V_{BATT_REG}, the charge current begins to decrease. The charge cycle is considered as completed when CV loop dominated and the charge current drops below the charge termination current threshold for 200ms deglitch time. Also a 200ms deglitch time is designed for starting each charge cycle, after 200ms expires the charge full signal will be allowed to assert if termination condition are met.



(a) Force Charge Time



(b) Termination Deglitch Time

Figure 4 Force Charge Time and Termination Deglitch Time

If I_{TERM} is not reached before the safety charge timer expires (***see Safety Timer section***), the charge cycle is ceased and corresponding timeout fault signal is asserted

A new charge cycle starts when the following conditions are valid:

- The input power is re-plugged
- Auto-recharge
- No thermistor fault at NTC pin.
- No safety timer fault.
- No battery over voltage.

The charge termination can be disabled manually by pulling NTC pin up to VCC.

Automatic Recharge

As shown in Figure 5, when the battery is charged full and the charging is terminated, the battery may be discharged for the system consumption or self-discharge. The MP2672 automatically starts another new charging cycle without the requirement of manually re-starting a charging cycle when battery voltage drops below the recharge threshold for 200ms.

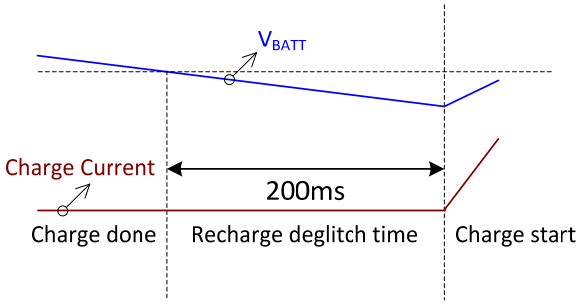


Figure 5 Recharge Profile

In case the battery is not expected to be charged frequently during high SOC condition, the MP2672 has an OTP option to disable charging when input power on and battery voltage is higher than recharge voltage threshold. The charging will be enabled till the battery voltage decreases below the recharge threshold.

Battery Full Voltage Setting

The MP2672 has a CV pin to program the battery regulation voltage.

When CV pin is pulled up to VCC, MP2672 operates in host-control mode. The battery regulation voltage is programmed through I^2C.

When CV pin is connected to AGND via a resistor, MP2672 operates in standalone mode. The battery regulation voltage is set according to below table.

Table 2: V_{BATT_REG} VS R_{VBATT} Resistor

Resistor Range	V_{BATT_REG}
30kΩ	8.4V
75kΩ	8.6V
105kΩ	8.7V
135kΩ	8.8V

Charge Current Setting

In standalone mode, the charge current is programmable via ISET pin. The setting formula is shown as below.

$$I_{CC} = \frac{12k\Omega}{R_{ISET}} (A) \quad (1)$$

In host mode, the charge current can be programmed via REG01H Bit [3:0] together with R_{ISET}. The R_{ISET} determines the full scale value of the register, for example

If R_{ISET} is 6kΩ, REG01H Bit [3:0] programmable range is 500mA to 2000mA with 100mA per step.

If R_{ISET} is 24kΩ, REG01G Bit [3:0] programmable range is 125mA to 500mA with 25mA per step.

R_{ISET} is recommended to be within 6kΩ− 24kΩ.

Minimum Input Voltage Limit

To avoid overloading the adapter, the MP2672 has the input voltage based power management by continuously monitoring the

input voltage. When the minimum input voltage limit is reach the charge current will be reduced to prevent the input voltage from dropping further. The minimum input voltage limit can be programmable by resistive divider at VLIM pin.

The internal reference of the input voltage loop is 1.2V, and the minimum input voltage limit can be set as below formula,

$$V_{IN\_MIN}=1.2\times\frac{R_H+R_L}{R_L} \quad (2)$$

Battery Supplement Mode and Ideal Diode Mode

As mentioned in last section, when minimum input voltage limit is hit, the charge current is reduced to keep the input voltage not dropping further. But when the charge current is reduce to zero and the input source is still overloaded due to heavy system load, the system voltage will continued dropping. Once the system voltage falls below the battery voltage, the MP2672 enters battery supplement mode. The battery starts to supplement the system load together with boost converter. During the supplement mode, the battery FET operates as an ideal diode.

When the system voltage falls 30 mV below the battery voltage, the battery FET turns on and its source to drain voltage is regulated at 24mV. As the battery discharge current goes higher the ideal diode loop will be saturated and the battery FET will be fully turned on. The source to drain voltage will be discharge current times the on resistance of battery FET.

Battery Missing Detection

The MP2672 is capable of detecting whether a battery is connected or not. The following conditions initiate battery missing detection:

- Charging is enabled.
- Auto-recharge is triggered.
- Recovery from any Faults

If battery absent is detected, Blinking at 1Hz indicates at STAT pin, BATTFLOAT_STAT is set 1 in host-control mode. Figure 6 shows the battery missing detection flow chart.

Battery Over-Voltage Protection

The MP2672 is designed with a built-in battery over voltage protection threshold, which is 104% of the V_{BATT_REG}. When the battery over voltage event occurs, the MP2672 turns off the battery FET (Q3) and suspends the charging. At this time the boost converter keeps operating and

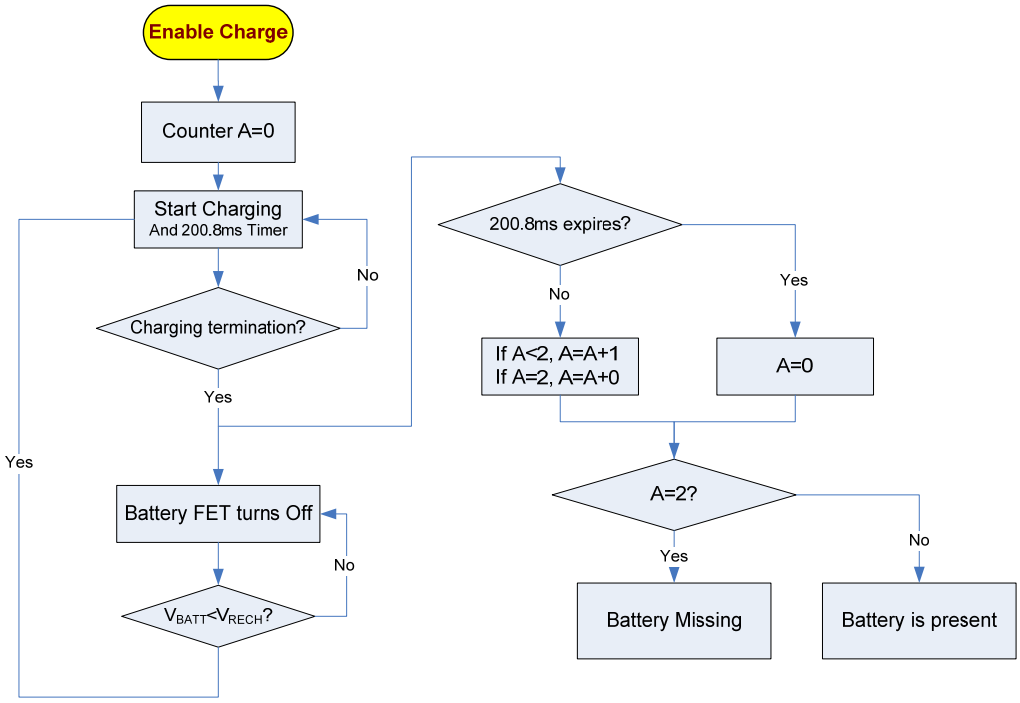


Figure 6 Battery Missing Detection Flow chart

system voltage tracks the battery voltage with additional V_{TRACK}.

MP2672 also has a MID pin to monitor each cell voltage. If any one of the cell voltages exceeds 104% of $V_{BATT\_REG}/2$, MP2672 also stop charging the battery.

Safety Timer

The MP2672 provides both pre-charge and fast charge cycle safety timer to avoid extended charging cycle due to abnormal battery conditions. The safety timer for pre-charge is 30 minutes when battery is lower than V_{BATT_PRE}. The fast charge cycle safety timer starts when the battery enters fast charge phase. The fast charge safety timer can be programmed by I^2C. The safety timer feature can also be disabled via I^2C.

The safety timer is reset at the beginning of a new charging cycle. Also it can be reset by writing 0 and 1 sequentially to the REG00 Bit4. The following actions restart the safety timer:

- A new charge cycle has begun.
- Write REG00 Bit4 from 0 to 1 (charge enable)
- Write REG02 Bit[2:1] from 00 to 01/10/11 (safety timer enable)
- Write REG02 Bit3 from 0 to 1 (software reset)

The timer is suspended during the conditions below:

- NTC hot or cold fault

In the event of the NTC hot and cold fault, the charging timer will be suspended. Once the NTC fault is removed, the timer will continue to count from the value before NTC fault.

If the input voltage regulation, or thermal regulation threshold is reached, the rest of the timer will be doubled if REG02 Bit0 is set to 1. Once the events above quit, the rest of the timer returns to the original setting.

Watchdog Timer

When MP2672 operates in host-control mode, a watchdog timer is provided to reset all the registers to default value if the watchdog timer is not reset periodically. By doing this the register value of MP2672 will go back to default when no action on I^2C bus for a certain time. The watchdog timer duration can be programmable and disabled through register.

NTC (Negative Temperature Coefficient) Thermistor

"Thermistor" is the generic name given to thermally sensitive resistors. Negative temperature coefficient thermistor is generally called as thermistor. Depending on the manufacturing method and the structure, there are many shapes and characteristic for various purposes. The thermistor resistance values, unless otherwise specified, are classified at a standard temperature of 25ºC. The resistance of a temperature is solely a function of its absolute temperature

Refer to datasheet of the thermistor, the mathematic expression which relates the resistance and the absolute temperature of a thermistor is shown in Equation.

$$R_1 = R_2 \times e^{\beta \bullet \left(\frac{1}{T1} - \frac{1}{T2}\right)} \quad (3)$$

Where: R1 is the resistance at absolute temperature T1, R2 is the resistance at absolute temperature T2 and β is a constant which depends on the material of the thermistor.

The MP2672 continuously monitors battery's temperature by measuring the voltage at the NTC pins. This voltage is determined by the resistive divider whose ratio produced by different resistance of the NTC thermistor under different ambient temperature of the battery.

MP2672 internally sets a pre-determined upper and lower bound of the range. If the voltage at the NTC pin goes out of hot/cold threshold which means the temperature is outside safe operating limit. At this time, the charging is ceased unless the operating temperature returns into the safe range.

To satisfy the JEITA requirement, the MP2672 monitors four temperature threshold, the cold battery threshold (e.g.T_{NTC}<0ºC), the cool battery threshold (e.g. 0ºC<T_{NTC}<10ºC), the warm battery threshold (e.g. 45ºC<T_{NTC}<60ºC), and the hot battery threshold (e.g. T_{NTC}>60ºC). For given NTC thermistor, these temperatures correspond to the V_{COLD}, V_{COOL}, V_{WARM}, and V_{HOT}. When V_{NTC}<V_{HOT} or V_{NTC}>V_{COLD}, the charging is suspended and timers are suspended.

When $V_{HOT}<V_{NTC}<V_{WARM}$, the battery regulation voltage V_{BATT_REG} is reduced by 140mV from the programmable threshold.

When $V_{COOL}<V_{NTC}<V_{COLD}$, the charging current is reduced to half of the programmable charge current.

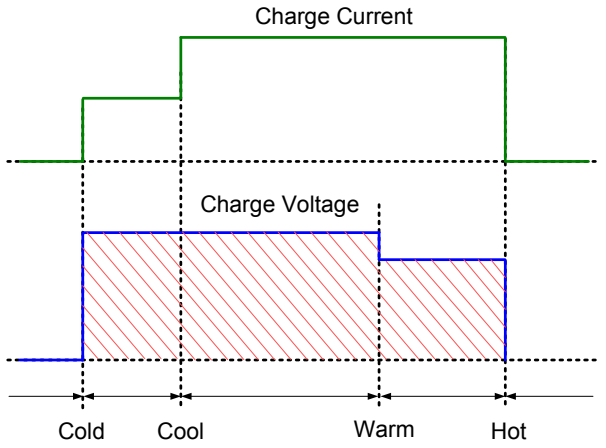


Figure 7 JEITA Compatible NTC Window

As Figure 8, given a thermistor is selected, two of four temperature thresholds can be programmable via changing values of R_{T1} and R_{T2}.

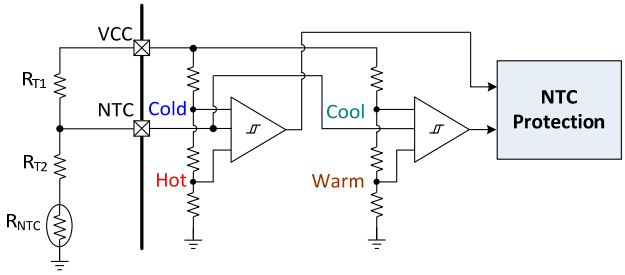


Figure 8 Diagram of NTC Protection Circuit

Thermal Regulation and Thermal Shutdown

To guaranteed safe operation, the MP2672 limits the die temperature to a preset value 120°C. When the internal junction temperature reaches the preset threshold, the MP2672 starts to reduce the charge current to prevent higher power dissipation. When the junction temperature reaches 150°C, the step-up converter goes into shutdown mode.

Indications

MP2672 has two open-drain pins $\overline{ACOK}$ and $\overline{STAT}$ to indication the input power and charging status. The behavior is shown in table 3.

Table 3 Indication in Difference Cases

Charging State	$\overline{ACOK}$	$\overline{STAT}$
In charging	Low	Low
Charging complete, charge disable	Low	Open-drain
Charge Suspended due to, • Battery OVP, • Timer Fault • NTC fault • Battery Float	Low	Blinking at 1Hz
Thermal Shutdown	Low	Open-drain

Battery Cell Balance and Protection

The MP2672 also provides the battery cell balance and protection for 2-cell application. It is able to sense the voltage across each cell, once these two cell voltages mismatch more than 50mV typically, the internal discharge path is turned on to discharge the cell of higher voltage until the two cell voltages match smaller than 30mV.

In case the battery OVP happens before the two cells are equalized, the charging will be suspended.

The MP2672 integrates the balance path and control circuit. An external power dissipation resistor is also required to limit the balance current.

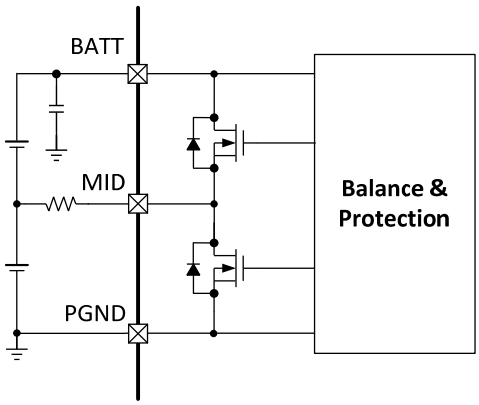


Figure 9 Block Diagram of the Battery Balance

Balancing Algorithm:

1. Balance block only operate in charging status.
2. Balance starts when any cell voltage is higher than balance start point V_{CELL_BAL}.
3. The voltage difference between cells should be higher than V_{CELL_DIFF}. The

4. MP2672 detects the cell with lower voltage in the pack, and then checks the voltage difference between each cell. If the differential voltage is higher than V_{CELL_DIFF}, the corresponding balance MOSFET is turned on.

To measure the open-circuit voltage of the cell, balancing will be suspended frequently for a short duration. Charging will always operate independent of balance algorithm if no other charge fault happens.

1. Measure for 200μs, balance for 249.8ms per each 250ms cycle

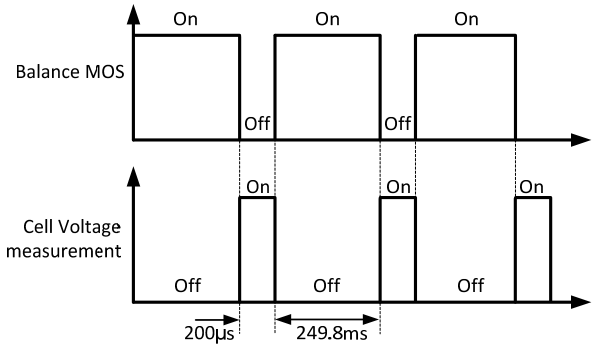


Figure 10 Clock of the Battery Balance

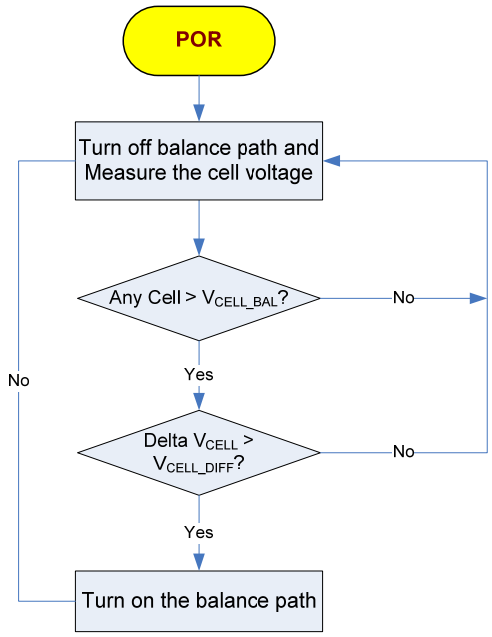


Figure 11 Flow chart of the Battery Balance

For extremely unbalanced 2-cell batteries, the charger takes a few cycles to make two battery voltages balanced. For some applications, like removable dual cell batteries, a charger is required to balance dual cells in one charge cycle. In this case, the circuit shown in Figure 12 is recommended.

The MP2672 also has an option to automatically disable the termination if the cell balance is active. By doing this the two cells will be matched better when charging terminated.

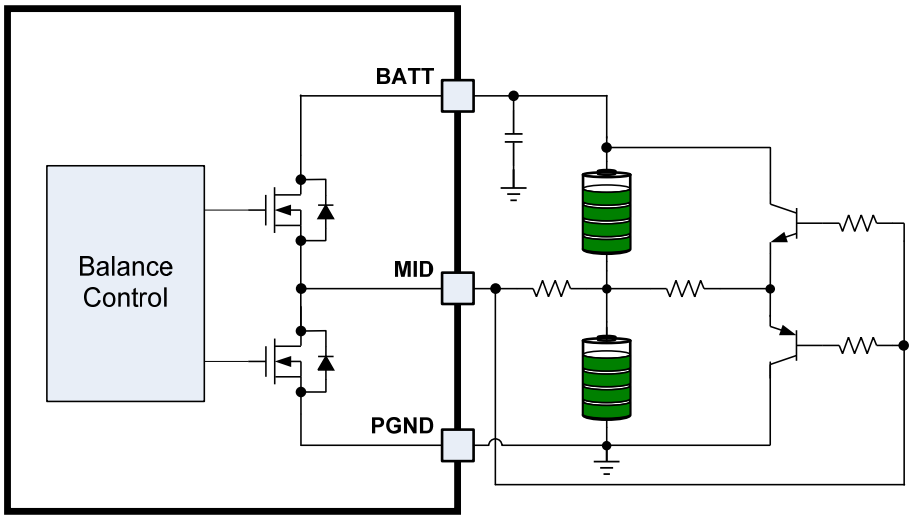


Figure 12 External Cell balance circuit

Series Interface

The IC uses an I²C compatible interface for flexible charging parameters setting and instantaneous device status reporting. I²C™ is a bidirectional 2-wire serial interface developed by Philips Semiconductor (now NXP Semiconductors). Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). The device can be considered a master or a slave when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit the transfer. At that time, any device addressed is considered as a slave.

The device operates as a slave device with the address 4BH, receiving control inputs from the master device, like a micro controller or a digital signal processor.

The I²C interface supports both standard mode (up to 100kbits), and fast mode (up to 400kbits). Both SDA and SCL are bi-direction lines, connecting to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

The Data on the SDA lint must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

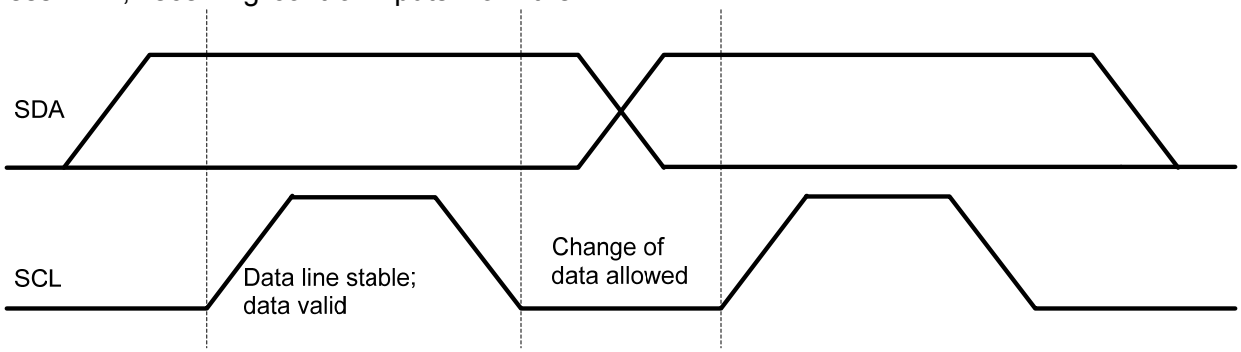


Figure 13: Bit Transfer on the I2C Bus

All the transactions begin with a START(S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA lint while SCI is HIGH defines a START condition. A LOW to HIGH transition on the SDA lint when the SCL is HIGH defines a STOP condition. START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

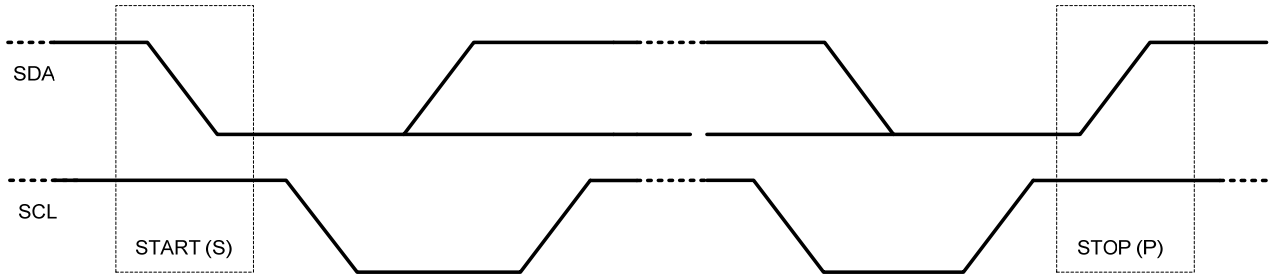


Figure 14: START and STOP Conditions

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

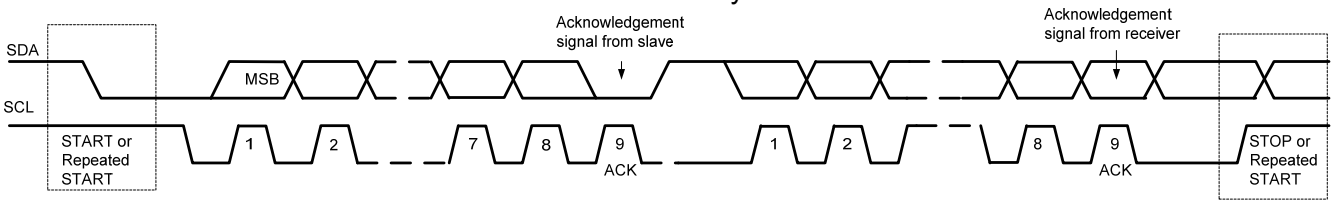


Figure 15: Data transfer on the I2C BUS

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

After the START, a slave address is sent, this address is 7 bits long followed by the 8th a data direction bit (bit R/W), A zero indicates a transmission (WRITE) and a one indicates a request for data (READ). The complete data transfer is shown in Figure 15.

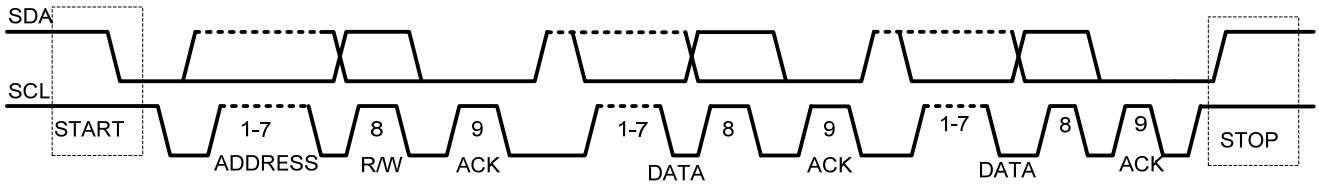


Figure 16: Complete Data Transfer

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

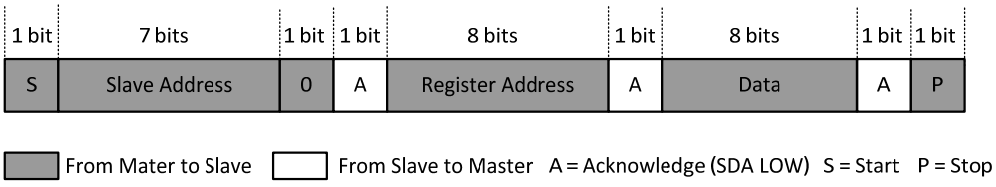


Figure 17: Single Write

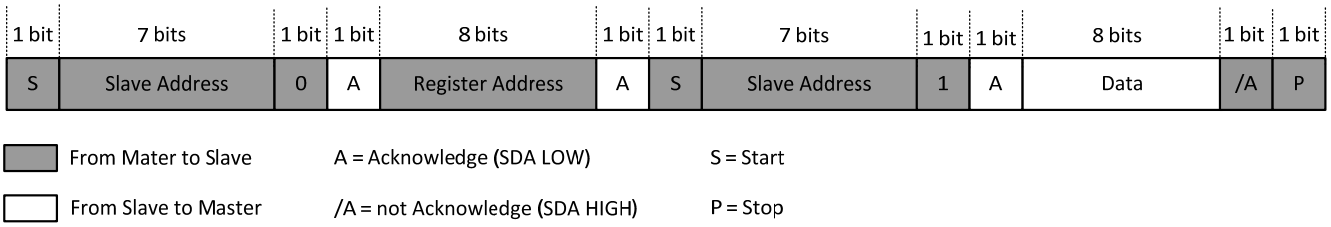


Figure 18: Single Read

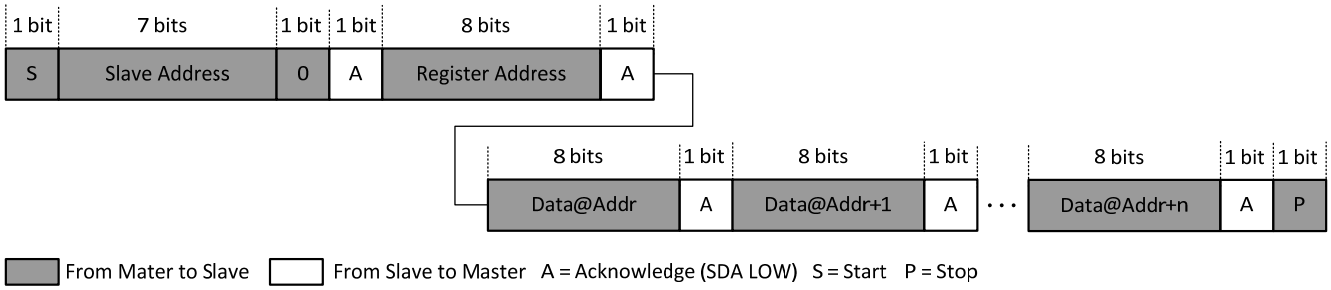


Figure 19: Multi Write

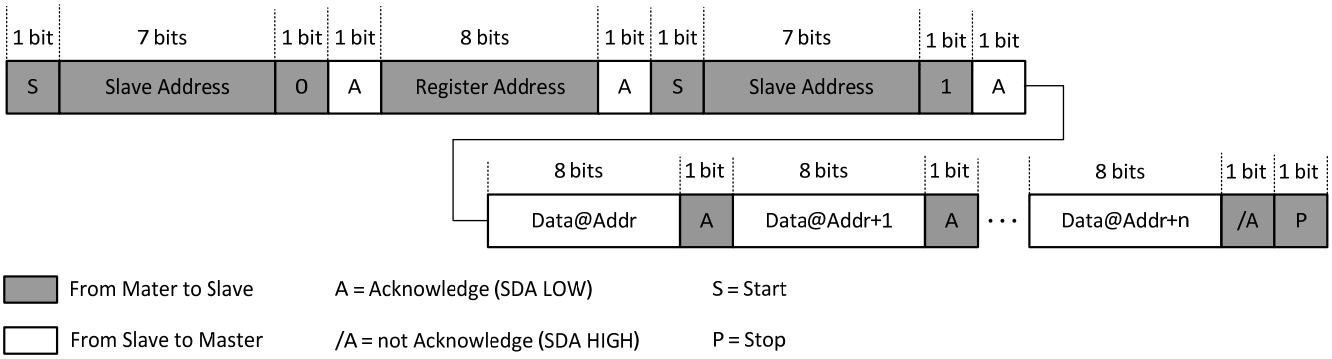


Figure 20: Multi Read

I²C Register MAP

IC Address 4BH

Register Name	Address	R/W	Description	Default
REG00	0x00	R/W	Battery regulation voltage, charge configure and SYS voltage setting	0011 1000
REG01	0x01	R/W	Balance setting and charge current setting	1000 1111
REG02	0x02	R/W	Timer setting	1001 0101
REG03	0x03	R	Status register	0000 0000
REG04	0x04	R	Fault register	0000 0000

REG 00H (Default: 0011 1000)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	V_{BATT_REG} [2]	0	Y	Y	R/W	000 – 8.3V 001 – 8.4V 010 – 8.5V 011 – 8.6V 100 – 8.7V 101 – 8.8V 110 – 8.9V 111 – 9.0V	**Battery Regulation Voltage** Default: (8.4V) OTP Programmable.
6	V_{BATT_REG} [1]	0	Y	Y	R/W		
5	V_{BATT_REG} [0]	1	Y	Y	R/W		
4	CHG CONFIG	1	Y	Y	R/W	0 – Charge Disable 1 – Charge Enable	Default: (charge Enable)
3	V_{BATT_PRE} [2]	1	Y	N	R/W	0.4V	**System Minimum Voltage Offset** Offset: 6.0V Range: 6.0V – 6.7V Default: 6.4V This threshold is also used as the per-charge battery voltage threshold. OTP Programmable
2	V_{BATT_PRE} [1]	0	Y	N	R/W	0.2V	
1	V_{BATT_PRE} [0]	0	Y	N	R/W	0.1V	
0	V_{TRACK}	0	Y	N	R/W	0 – 200mV 1 – 300mV	**Battery Track Voltage** Default: 200mV

REG 01H (Default: 1000 1111)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	NTC_TYPE	1	Y	Y	R/W	0 – Standard 1 – JEITA	Default: JEITA. OTP programmable.
6	V_{CELL_BAL}	0	Y	Y	R/W	0 - 3.5V 1 - 3.7V	**Cell Balance Start Point** Default: 3.5V OTP programmable.
5	Balance Threshold_H2L	0	Y	Y	R/W	0 - 50mV 1 - 70mV	**Cell Balance threshold** Default: 50mV OTP programmable.
4	Balance Threshold_L2H	0	Y	Y	R/W	0 - 50mV 1 - 70mV	**Cell Balance threshold** Default: 50mV OTP programmable.
3	I_{CC} [2]	1	Y	Y	R/W	800mA	**Fast Charge Current Setting** If R_{ISET} is 6kΩ Offset: 500mA Range: 500mA – 2000mA Default: 2000mA (1111) If R_{ISET} is 24kΩ Offset: 125mA Range: 125mA – 500mA Default: 500mA (1111) OTP programmable.
2	I_{CC} [2]	1	Y	Y	R/W	400mA	
1	I_{CC} [1]	1	Y	Y	R/W	200mA	
0	I_{CC} [0]	1	Y	Y	R/W	100mA	

REG 02H (Default: 1001 0101)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	FSW	1	Y	Y	R/W	0 – 600kHz 1 – 1200kHz	Default: (1)1200kHz OTP Programmable
6	I^2C WD Timer Reset	0	Y	N	R/W	0 – Normal 1 – Reset	Default: 0 (Normal)
5	WD Timer [1]	0	Y	N	R/W	00 – Disable timer 01 – 40s 10 – 80s 11 – 160s	**I^2C WD Timer Limit** Default: 40s (01) OTP programmable.
4	WD Timer [0]	1	Y	N	R/W		
3	Register Reset	0	Y	N	R/W	0 - Keep current setting 1 - Reset	Default: 0 After Reset, this bit go back to 0 automatically
2	CHG_TMR [1]	1	Y	Y	R/W	00 – Disable CHG Timer 01 – 8 hrs 10 – 12 hrs 11 – 20 hrs	Default: 10 (12 hrs)
1	CHG_TMR [0]	0	Y	Y	R/W		
0	TMRX2_EN	1	Y	Y	R/W	0 – Disable 2x extended safety timer 1 – Enable 2x extended safety timer	Default: 1 (Enable)

REG 03H (Default: 0000 0000)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	Reserved	NA	NA	NA	R	Reserved	Reserved
6	Reserved	NA	NA	NA	R	Reserved	Reserved
5	CHG_STAT [1]	0	NA	NA	R	00 – Not charge 01 – Pre charge 10 – constant-current charge 11 – charge done	Default: 00
4	CHG_STAT [0]	0	NA	NA	R		
3	PPM_STAT	0	NA	NA	R	0 – Not PPM 1 – VINPPM	Default: 0
2	BATTFLOAT_STAT	0	NA	NA	R	0 – Battery present 1 – Battery missing	Default: 0
1	THERM_STAT	0	NA	NA	R	0 – Normal 1 – Thermal regulation	Default: 0
0	VSYS_STAT	0	NA	NA	R	0 – Not in VSYSMIN regulation 1 – In VSYSMIN regulation	Default: 0

REG 04H (Default: 0000 0000)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	WD_FAULT	0	NA	NA	R	0 - Normal 1 - WD Timer Expiration	Default: 0
6	INPUT_FAULT	0	NA	NA	R	0 - Normal 1 - Input fault (OVP)	Default: 0
5	THERM SD_FAULT	0	NA	NA	R	0 – Normal 1 – Thermal shutdown	Default: 0
4	TIMER_FAULT	0	NA	NA	R	0 – Normal 1 – Safety timer expiration	Default: 0
3	BAT_FAULT	0	NA	NA	R	0 – Normal, 1 – Battery OVP,	Default: 0
2	NTC_FAULT [2]	0	NA	NA	R	000 – Normal 001 – NTC cold 010 – NTC cool 011 – NTC warm 100 – NTC hot	Default: 000
1	NTC_FAULT [1]	0	NA	NA	R		
0	NTC_FAULT [0]	0	NA	NA	R		

REG 05H (Default: 1110 0000)(6)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RCHG	1	NA	NA	NA	0 – No charging after input power on when $V_{BATT} > V_{RECH}$. 1 – Automatic charging after input power on when $V_{BATT} > V_{RECH}$.	Default: 1
6	Reserved	NA	NA	NA	NA	Reserved	
5	BALANCE_EOC_EN	1	NA	NA	NA	0 – Not Suspend termination when cell balance is active 1 – Suspend termination when cell balance is active	Default: 1
4	T_{J_REG} [1]	0	NA	NA	NA	00 - 120ºC 01 - 100ºC 10 - 80ºC 11 - 60ºC	Default:00
3	T_{J_REG} [0]	0	NA	NA	NA		
2	Reserved	NA	NA	NA	NA	Reserved	Reserved
1	Reserved	NA	NA	NA	NA	Reserved	Reserved
0	Reserved	NA	NA	NA	NA	Reserved	Reserved

Notes:
6) This register is for OTP only and not accessible to customers.

OTP MAP

#	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00	V_{BATT_REG}: 8.3V-9.0V			N/A	V_{BATT_PRE}: 6.0V-6.7V			N/A
01	NTC Type	V_{CELL_BAL}	$V_{CELL\_DIFF\_HL}$	$V_{CELL\_DIFF\_LH}$	I_{CC}: 500mA-2000mA/100mA step (R_{ISET}=6kΩ)			
02	FSW	N/A	WATCHDOG		N/A	N/A	N/A	N/A
05*	RCHG	N/A	BALANCE_EOC_EN	T_{J_REG}: 60/80/100/120ºC		N/A	N/A	N/A

*Note: REG05 is for OTP only, cannot be accessible to customer.

OTP DEFAULT

OTP Items	Default
V_{BATT_REG}	8.4V
V_{BATT_PRE}	6.4V
NTC Type	JEITA
V_{CELL_BAL}	3.5V
Balance Threshold H2L	50mV
Balance Threshold L2H	50mV
I_{CC}	2000mA
SW FREQ	1200kHz
WATCHDOG	40s
RCHG	New charge cycle starts when V_{BATT}> V_{RECH} after power on.
BALANCE_EOC_EN	Enable (if two cell is not balanced, EOC is not asserted even all conditions are met)
Thermal Regulation Threshold	120ºC

APPLICATION INFORMATION

Setting the Charge Current in Standalone Mode

In standalone mode, the charge current of the MP2672 can be set by an external resistor (R_{ISET}) in according to Equation (4):

$$I_{CC}=\frac{12k\Omega}{R_{ISET}}(A) \quad (4)$$

The charge current can be programmed up to 2.0A. The expected R_{ISET} for a typical charge current is shown in Table 4.

Table 4: Charge Current Setting Table

R_{ISET} (kΩ)	I_{CC} (A)
24	0.5
12	1
6	2.0

In host-control mode, the R_{ISET} determines the full-scale current when I_{CC} [3:0] is set to all 1.

Setting the Input Minimum Voltage Limit

In charge mode, connect a resistor divider from IN to AGND tapped to VLIM to program the input minimum voltage using Equation (5):

$$V_{IN\_MIN}=1.2V\times\frac{R_H+R_L}{R_L} \quad (5)$$

Where 1.2V is the reference of the input minimum voltage loop. With given R_L, R_H can be calculated as below,

$$R_H=R_L\times\frac{V_{IN\_MIN}-1.2V}{1.2V} \quad (6)$$

For example, assume 4.675V input minimum voltage limit is expected, R_L=10kΩ and R_H=27.4kΩ would be one of the choices.

Resistor Selection for the NTC Sensor

Figure 6 shows an internal resistor divider reference circuit that limits both the high and low temperature thresholds at V_{HOT} and V_{COLD} respectively. For a given NTC thermistor, select appropriate R_{T1} and R_{T2} to set the NTC window.

$$R_{T2}=\frac{R_{NTC\_HOT}\bullet V_{COLD}\bullet(1-V_{HOT})-R_{NTC\_COLD}\bullet V_{HOT}\bullet(1-V_{COLD})}{V_{HOT}-V_{COLD}} \quad (7)$$

$$R_{T1}=\frac{(1-V_{COLD})\times(R_{NTC\_COLD}+R_{T2})}{V_{COLD}} \quad (8)$$

R_{NTC_HOT} is the value of the NTC resistor at high temperature of the required temperature operation range, and R_{NTC_COLD} is the value of the NTC resistor at low temperature.

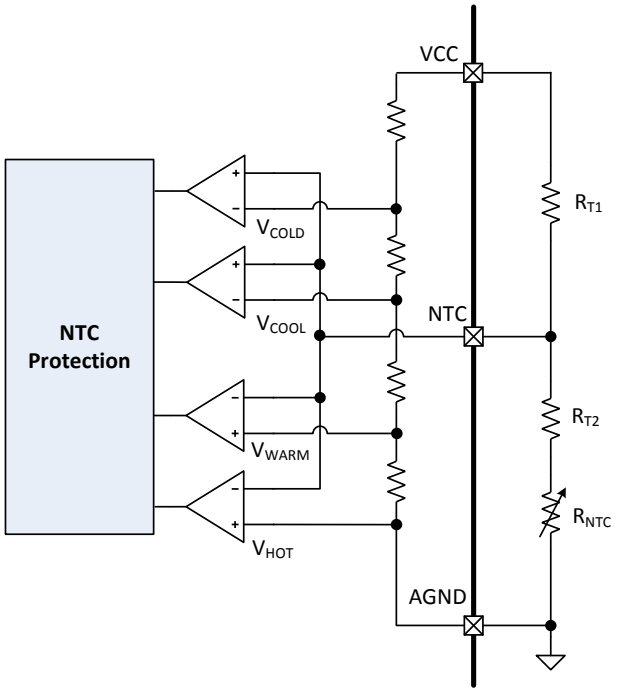


Figure 21 NTC Protection Block

R_{T1} and R_{T2} allow the high temperature limit and low temperature limit to be programmed independently.

With this feature, the MP2672 can fit most type of NTC resistor and different temperature operation range requirements.

R_{T1} and R_{T2} values depend on the type of the NTC resistor.

For example, for the 103AT thermistor, it has the following electrical characteristic:

At 0°C, R_{NTC_COLD} = 27.28kΩ;

At 60°C, R_{NTC_HOT} = 3.02kΩ.

According to the above equations (7) and (8), V_{HOT} and V_{COLD} from the EC table to calculate R_{T1}=12.78kΩ and R_{T2}=3.71kΩ.

Please apply spreadsheet about R_{T1} and R_{T2} calculation if required.

Selecting the Inductor

Inductor selection is a trade-off between cost, size and efficiency. A lower inductance value results in lower DCR for same component size, but results in higher current ripple, higher magnetic hysteretic losses, and higher output capacitances. From a practical standpoint, the inductor ripple current does not exceed 30% of maximum input current under worst case conditions.

Choose an inductor that does not saturate under the worst-case load condition. The saturate current of inductor should be higher than peak current limit of low-side FET.

When the MP2672 works in charge mode, estimate the required inductance with Equation (9), Equation (10) and Equation (11):

$$L=\frac{V_{IN}\bullet(V_{SYS}-V_{IN})}{V_{SYS}\bullet F_{SW}\bullet\Delta I_{L\_MAX}} \quad (9)$$

$$\Delta I_{L\_MAX}=2\times\left(I_{L\_PK}-I_{IN(MAX)}\right) \quad (10)$$

Where V_{SYS} is the system minimum regulation voltage, F_{SW} is the switching frequency, ΔI_{L_MAX} is the peak-to-peak inductor ripple current, $I_{IN(MAX)}$ is maximum input current and I_{L_PK} is the expected inductor peak current.

In the case with a 9V battery voltage, 3.3A maximum input current, typical input voltage (V_{IN}=5V), 1.2MHz switching frequency and expected 4.5A inductor peak current, the inductance is calculated as 1μH.

Then a 1μH with > 5A saturation current is recommended for 1.2MHz switching frequency. And 1.5μH-2.2μH with >5A saturation current is recommended for 600kHz switching frequency.

Selecting the Input Capacitor

C_{IN} is the input capacitor of the boost converter during charge mode. Calculate its values with Equation (12) and Equation (13):

$$\frac{\Delta V_{IN}}{V_{IN}}=\frac{1-V_{IN}/V_{SYS}}{8\bullet C_{IN}\bullet F_{SW}{}^{2}\bullet L} \quad (12)$$

$$C_{IN}=\frac{1-V_{IN}/V_{SYS}}{8\bullet F_{SW}{}^{2}\bullet L\bullet\Delta V_{IN}/V_{IN}} \quad (13)$$

Assume maximum input voltage ripple is 1%. When V_{SYS} is 9.3V, V_{IN} is 5V, L is 1μH, F_{SW} is 1200kHz, then C_{IN} is 4.7μF.

Place one 4.7μF ceramic capacitor with X5R or X7R at IN terminal.

Selecting the System Capacitor

In charge mode, the capacitor C_{SYS} is the output capacitor of the boost converter. C_{SYS} keeps the V_{SYS} ripple small (<0.5%) and ensures feedback loop stability. Select the system capacitors base on the ripple current. For best results, use X5R or X7R dielectric ceramic capacitors with low ESR and small temperature coefficients. For most applications, place two 22μF capacitors and one 1μF capacitor as close to the IC as possible.

PCB Layout Guidelines

Efficient PCB layout is critical for meting specified noise, efficiency, and stability requirements. For best results, follow the guidelines below.

1. Route the power stage adjacent to their grounds.
2. Minimize the length of high-side switching node (SW, inductor) trace that carries the high current.
3. Keep the switching node short and away from all control signals, especially the feedback network.
4. Place the input capacitor as close to VSYS and PGND as possible.
5. Place the local power input capacitors connected from VIN to PGND as close as possible.
6. Place the output inductor close to the IC.

TYPICAL APPLICATION CIRCUITS

Point-of-sale (POS) Machine
Figure TBD

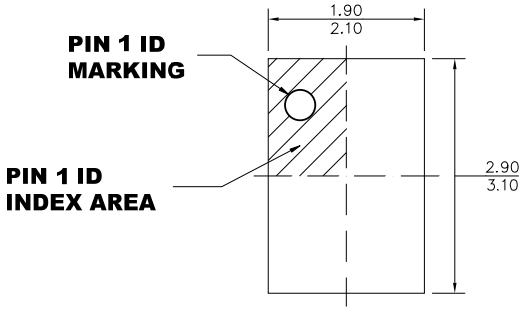
Blue-tooth Speaker
Figure TBD

E-cigarette
Figure TBD

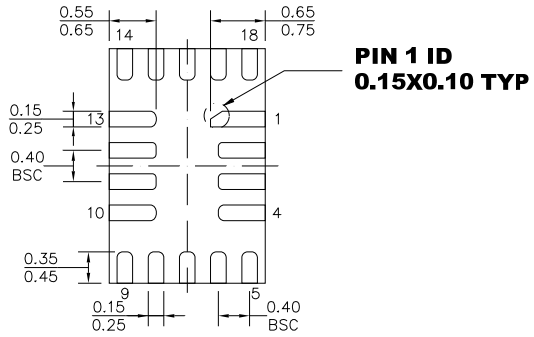
Handheld Gimbal
Figure TBD

PACKAGE INFORMATION

QFN-18 (2mmX3mm)

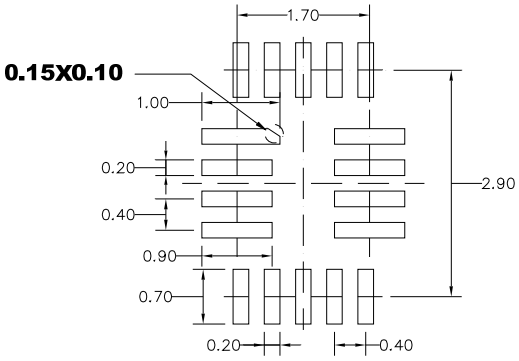


TOP VIEW



BOTTOM VIEW

SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.